Hex AND Gate

The MC10197 provides a high speed hex AND function with strobe capability.

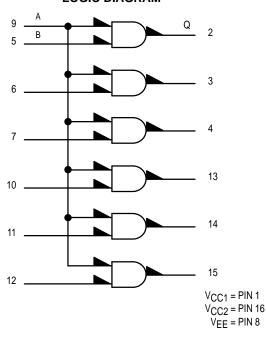
P_D = 200 mW typ/pkg (No Load)

 $t_{pd} = 2.8 \text{ ns typ (B-Q)}$

 $t_{pd} = 3.8 \text{ ns typ } (A-Q)$

 t_r , $t_f = 2.5$ ns typ (20%–80%)

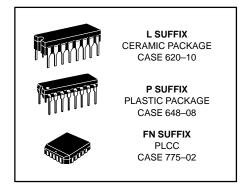
LOGIC DIAGRAM



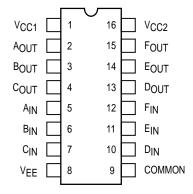
TRUTH TABLE

Inp	uts	Output		
Α	В	Q		
L	L	L		
L	Н	L		
Н	L	L		
Н	Н	Н		

MC10197



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

ELECTRICAL CHARACTERISTICS

		Test Limits								
		Pin Under	−30°C		+25°C			+85°C		1
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current	ΙΕ	8		54		39	49		54	mAdc
Input Current	l _{inH}	5 9		425 460			265 290		265 290	μAdc
	linL	5	0.5		0.5		0.3			μAdc
Output Voltage Logic 1	Voн	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage Logic 0	VOL	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage Logic 1	Vона	2	-1.080		-0.980			-0.910		Vdc
Threshold Voltage Logic 0	VOLA	2		-1.655			-1.630		-1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t ₅₊₂₊ t ₉₊₂₊	2 2	1.1 1.1	4.2 5.3	1.1 1.1	2.8 3.5	4.0 5.0	1.1 1.1	4.4 5.5	
Rise Time (20 to 80%)	t ₂₊	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	t ₂₋	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	

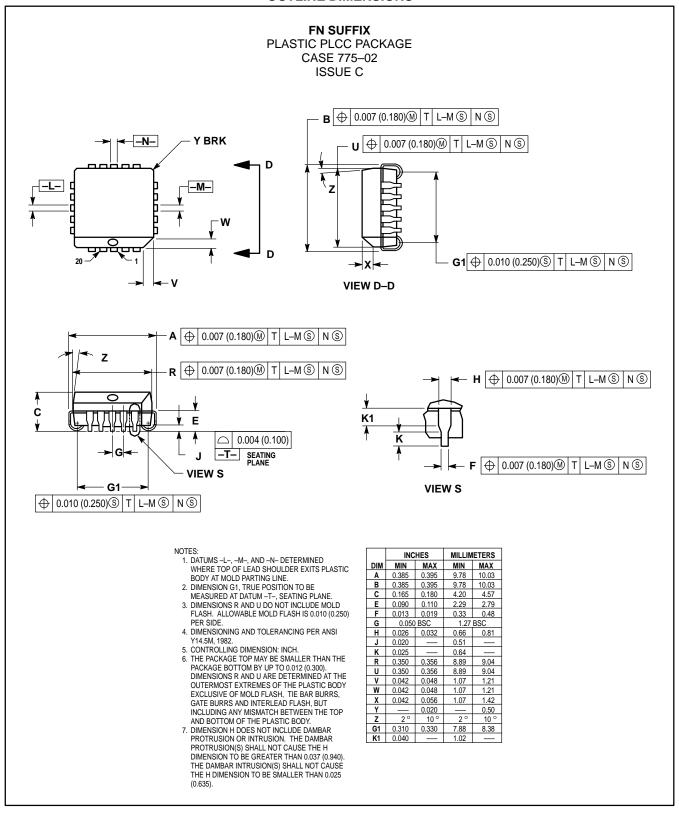
ELECTRICAL CHARACTERISTICS (continued)

					TEST VOI	LTAGE VALU	JES (Volts)		
		@ Test Te	mperature	V _{IHmax}	V _{ILmin}	VIHAmin	V _{ILAmax}	VEE	
	–30°C			-0.890	-1.890	-1.205	-1.500	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
			Pin	TEST V	TEST VOLTAGE APPLIED TO PINS LISTED BELOW				
Characteristic		Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	VEE	(VCC)
Power Supply Drain Current		lΕ	8					8	1, 16
Input Current		l _{inH}	5 9	5 9				8 8	1, 16 1, 16
		l _{inL}	5		5			8	1, 16
Output Voltage	Logic 1	VOH	2	5, 9				8	1, 16
Output Voltage	Logic 0	VOL	2					8	1, 16
Threshold Voltage	Logic 1	Vона	2	9		5		8	1, 16
Threshold Voltage	Logic 0	V _{OLA}	2	9			5	8	1, 16
Switching Times	(50Ω Load)				+1.11V	Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay		^t 5+2+ t9+2+	2 2		9 5	5 9	2 2	8 8	1, 16 1, 16
Rise Time	(20 to 80%)	t ₂₊	2		9	5	2	8	1, 16
Fall Time	(20 to 80%)	t ₂₋	2		9	5	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

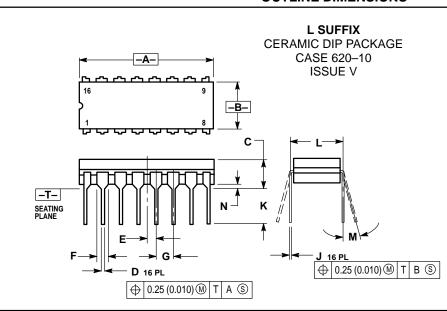
3–169 MOTOROLA

OUTLINE DIMENSIONS



MOTOROLA 3–170

OUTLINE DIMENSIONS

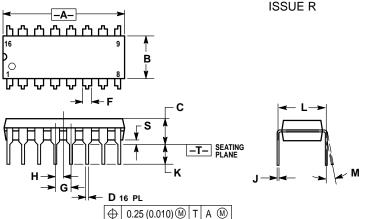


NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN	MIN MAX		MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	0.100 BSC		2.54 BSC	
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62 BSC		
М	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.015 0.021		0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

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